GP 2813 $

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Cabral et al.

Serial No.: 09/902,483 Group Art Unit: 2813

Filed: July 11, 2001 Examiner: Erik Kielin

For: SELF-ALIGNED SILICIDE (SALICIDE) PROCESS FOR LOW RESISTIVITY CONTACTS TO THIN FILM SILICON-ON-INSULATOR AND BULK MOSFETS AND FOR SHALLOW JUNCTIONS

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231

EXCESS CLAIM FEE PAYMENT LETTER

Sir:

Transmitted herewith is an amendment in the above-identified application. The fee has been calculated and is transmitted as shown below.

	AFTER AMENDMENT	PREV. PAID FOR	EXTRA CLAIMS PRESENT	RATE	FEE DUE
Total Claims	28 -	22	= 6	x $18.00	$ 108.00
Indep. Claims	6 -	6	= 0	x $84.00	$ 0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					**$ 108.00**

The Commissioner is authorized to charge Assignee's Deposit Account No. 50-0510 in the amount of $108.00 to cover the excess claim fees. A duplicate copy of this sheet is enclosed. The Commissioner is authorized to charge any deficiencies in fees and credit any overpayment of fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 1/2/03

Sean M. McGinn
Reg. No. 34,386

McGinn & Gibb, PLLC
Intellectual Property Law
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Cabral et al.

Serial No.: 09/902,483 Group Art Unit: 2813

Filed: July 11, 2001 Examiner: Erik Kielin

For: SELF-ALIGNED SILICIDE (SALICIDE) PROCESS FOR LOW RESISTIVITY CONTACTS TO THIN FILM SILICON-ON-INSULATOR AND BULK MOSFETS AND FOR SHALLOW JUNCTIONS

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated October 1, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

1. (Amended) A method for fabricating a silicide for a semiconductor device, said method comprising:

depositing a metal containing silicon or a metal alloy on a silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and